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10/797,941

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EXAMINER

RAHMAN, FAHMIDA

ART UNIT

PAPER NUMBER

2116

MAIL DATE

DELIVERY MODE

09/19/2007

PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

## Office Action Summary

Application No.

10/797,941

Applicant(s)

BACHA ET AL.

Examiner

Fahmida Rahman

Art Unit

2116

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 05 July 2007.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-21 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-21 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 11 March 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

### DETAILED ACTION

1. This final action is in response to communications filed on 7/5/2007.
2. Claims 1, 8, 14 have been amended, no new claims have been added and no claims have been canceled. Thus, claims 1-21 are pending.

### Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1 and 4 are rejected under 35 U.S.C. 102(b) as being anticipated by Ishibashi (US Patent 5420544).

For claim 1, Ishibashi teaches the following limitations:

**A circuit module (Fig 9) comprising: a circuit board (lines 35-36 of column 1); multiple circuit units on the circuit board (70A-70C are LSIs comprising internal circuits 71A-71C. Lines 45-60 of column 1 mention that the internal circuit 71A forms elements. Therefore, the elements comprising 71A-71C are the circuit units); at least one clock input (73) on the circuit board for receiving an external clock signal (line 41 of column 1 mentions that 73 is an external clock); a first phase locked loop (PLL) unit (72A) on the circuit board for providing an internal clock signal (75A) based on the external clock signal (73) to a first set of at least two of the circuit**

**units** (71A has plural elements mentioned in line 47 of column 1. Each element comprises one circuit unit. Thus, 71A has plural circuit units); **and a second PLL unit (72C) on the circuit board for providing an internal clock signal (75C) based on the external clock signal (73) to a second set of at least two of the circuit units** (lines 56-59 of column 1 mention that the steps similar to 70A are performed in 70C. Thus, 71C has plural elements that are fed with clock 75C), **wherein each circuit unit in the first set is provided with the internal clock signal from the first PLL unit and not from the second PLL unit and wherein each circuit unit in the second set is provided with the internal clock signal from the second PLL unit and not from the first PLL unit** (Fig 9 shows that 71A is provided from 72A and not from 72C and 71C is provided from 72C and not from 72A).

For claim 4, the PLL clock inputs are connected to the same clock input.

### **Claim Rejections - 35 USC § 103**

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 2-3, 5-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishibashi (US Patent 5420544), in view of Matsuzaki (US Patent Application Publication 2001/0050856).

For claims 2 and 3, Ishibashi does not teach that the circuit module is a memory module or PLL inputs are connected to different clock input.

Matsuzaki's circuit module is a memory module and units are memory chips ([0077]). PLL units have clock inputs that are connected to different clock inputs (CLK4, Fig 8) on the circuit board and also the same clock input on the circuit board (CLK, Fig 7).

It would have been obvious for one ordinary skill in the art at the time the invention was made to combine the teachings of Ishibashi and Matsuzaki. One ordinary skill would be motivated to include the memory chips of Matsuzaki in Ishibashi, since Ishibashi's teachings broadly covers LSI chips and memory module can be LSI chips.

For claim 5, 22 of Matsuzaki is the feedback loop for PLL1 and PLL2-25-p3-p2-PLL2 is the feedback loop for PLL2. Frequency of CLK2 is controlled by comparing CLK4 with CLK and CLK4 is transmitted over feedback loop (Fig 8, [0051]).

For claims 6 and 7, feedback loops of Matsuzaki are shared by two PLLs (21) and the feedback loops have input to both PLL. 25 and 23 of Fig 7 are the two branches of feedback loop.

5. Claims 8-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishibashi (US Patent 5420544), in view of Matsuzaki (US Patent Application Publication 2001/0050856), further in view of Kikuo Kuma (EP 0379592).

For claim 8, Ishibashi teaches the following limitations:

**A circuit module (Fig 9) comprising: a circuit board** (lines 35-36 of column 1); **multiple circuit units on the circuit board** (70A-70C are LSIs comprising internal circuits 71A-71C. Lines 45-60 of column 1 mention that the internal circuit 71A forms elements. Therefore, the elements comprising 71A-71C are the circuit units); **at least one clock input (73) on the circuit board for receiving an external clock signal** (line 41 of column 1 mentions that 73 is an external clock); **a first phase locked loop (PLL) unit (72A) on the circuit board for providing an internal clock signal (75A) based on the external clock signal (73) to a first set of at least two of the circuit units** (71A has plural elements mentioned in line 47 of column 1. Each element comprises one circuit unit. Thus, 71A has plural circuit units); **and a second PLL unit (72C) on the circuit board for providing an internal clock signal (75C) based on the external clock signal (73) to a second set of at least two of the circuit units** (lines 56-59 of column 1 mention that the steps similar to 70A are performed in 70C).

Thus, 71C has plural elements that are fed with clock 75C), **wherein each circuit unit in the first set is provided with the internal clock signal from the first PLL unit and not from the second PLL unit and wherein each circuit unit in the second set is provided with the internal clock signal from the second PLL unit and not from the first PLL unit** (Fig 9 shows that 71A is provided from 72A and not from 72C and 71C is provided from 72C and not from 72A).

Ishibashi does not mention that the circuit board is a memory module and memory module comprises multiple memory chips on the circuit boards.

Matsuzaki teaches the following limitations:

A circuit module (14 in Fig 7) comprising: a circuit board (160); a plurality of memory chips ([0077]) arranged along the width of the circuit board (120-127) comprising a first set of memory chips (120-123) and a second set of memory chips (124-127); at least one clock input on the circuit board for receiving an external clock signal ("CLK" in Fig 7); a first phase locked loop (PLL) unit (16) arranged within the first set of memory chips for providing an internal clock signal based on the external clock signal to at least one of the memory chips (120, 121); and a second PLL unit (15) arranged within said second set of memory chips for providing an internal clock signal based on the external clock signal to at least one of the memory chips (126, 127), wherein the second set and the first set are mutually exclusive (first set with 120 and 121, and second set with 126, 127 are mutually exclusive, since the two sets do not share any common module).

It would have been obvious for one ordinary skill in the art at the time the invention was made to combine the teachings of Ishibashi and Matsuzaki. One ordinary skill would be motivated to include the memory chips of Matsuzaki in Ishibashi, since Ishibashi's teachings broadly covers LSI chips and memory module can be LSI chips (Kikuo Kuma teaches a memory module (Fig 1) comprising a circuit board (2) and multiple LSI memory chips (6; lines 13-14 of page 6 and line 10 of page 7) reside on the circuit board (page 6)).

For claim 9, circuit module of Matsuzaki is a memory module and units are memory chips ([0077]). PLL units have clock inputs that are connected to different clock inputs (CLK4 in Fig 14) on the circuit board and also the same clock input (CLK, Fig 14) on the circuit board.

For claim 10, the PLL clock inputs are connected to the same clock input in Ishibashi.

For claim 11, 22 of Matsuzaki is the feedback loop for PLL1 and PLL2-25-p3-p2-PLL2 is the feedback loop for PLL2. Frequency of CLK2 is controlled by comparing CLK4 with CLK and CLK4 is transmitted over feedback loop (Fig 8, [0051]).

For claims 12 and 13, feedback loops are shared by two PLLs (21) and the feedback loops have input to both PLL (Fig 14). 25 and 23 of Fig 7 are the two branches of feedback loop in Matsuzaki.

For claim 14, Ishibashi teaches the following limitations:

**A circuit module (Fig 9) comprising: a circuit board (lines 35-36 of column 1); multiple circuit units on the circuit board (70A-70C are LSIs comprising internal circuits 71A-71C. Lines 45-60 of column 1 mention that the internal circuit 71A forms elements. Therefore, the elements comprising 71A-71C are the circuit units); at least one clock input (73) on the circuit board for receiving an external clock signal (line 41 of column 1 mentions that 73 is an external clock); a first phase locked loop (PLL) unit (72A) on the circuit board for providing an internal clock signal (75A) based on the external clock signal (73) to a first set of at least two of the circuit units (71A has plural elements mentioned in line 47 of column 1. Each element comprises one circuit unit. Thus, 71A has plural circuit units); and a second PLL unit (72C) on the circuit board for providing an internal clock signal (75C) based on the external clock signal (73) to a second set of at least two of the circuit units (lines 56-59 of column 1 mention that the steps similar to 70A are performed in 70C. Thus, 71C has plural elements that are fed with clock 75C), wherein each circuit unit in the first set is provided with the internal clock signal from the first PLL unit and not from the second PLL unit and wherein each circuit unit in the second set is provided with the internal clock signal from the second PLL unit and not from the**

**first PLL unit** (Fig 9 shows that 71A is provided from 72A and not from 72C and 71C is provided from 72C and not from 72A).

Ishibashi does not mention that the circuit board is a memory module and memory module comprises multiple memory chips on the circuit boards.

Matsuzaki teaches the following limitations:

A circuit module (14 in Fig 7) comprising: a circuit board (160); a plurality of memory chips ([0077]) arranged along the width of the circuit board (120-127) comprising a first set of memory chips (120-123) and a second set of memory chips (124-127); at least one clock input on the circuit board for receiving an external clock signal ("CLK" in Fig 7); a first phase locked loop (PLL) unit (16) arranged within the first set of memory chips for providing an internal clock signal based on the external clock signal to at least one of the memory chips (120, 121); and a second PLL unit (15) arranged within said second set of memory chips for providing an internal clock signal based on the external clock signal to at least one of the memory chips (126, 127), wherein the second set and the first set are mutually exclusive (first set with 120 and 121, and second set with 126, 127 are mutually exclusive, since the two sets do not share any common module).

It would have been obvious for one ordinary skill in the art at the time the invention was made to combine the teachings of Ishibashi and Matsuzaki. One ordinary skill would be motivated to include the memory chips of Matsuzaki in Ishibashi, since Ishibashi's

Art Unit: 2116

teachings broadly covers LSI chips and memory module can be LSI chips (Kikuo Kuma teaches a memory module (Fig 1) comprising a circuit board (2) and multiple LSI memory chips (6; lines 13-14 of page 6 and line 10 of page 7) reside on the circuit board (page 6)).

For claims 15 and 16, PLLs of Matsuzaki are approximately at the center.

For claims 17-18, circuit module of Matsuzaki is a memory module and units are memory chips ([0077]). PLL units have clock inputs that are connected to different clock inputs (CLK4 in Fig 14) on the circuit board and also the same clock input (CLK, Fig 14) on the circuit board.

For claim 19, 22 of Matsuzaki is the feedback loop for PLL1 and PLL2-25-p3-p2-PLL2 is the feedback loop for PLL2. Frequency of CLK2 is controlled by comparing CLK4 with CLK and CLK4 is transmitted over feedback loop (Fig 8, [0051]).

For claims 20 and 21, feedback loops are shared by two PLLs (21) and the feedback loops have input to both PLL (Fig 14). 25 and 23 of Fig 7 are the two branches of feedback loop in Matsuzaki.

### **Response to Arguments**

Applicant's arguments filed on 7/5/2007 have been fully considered but they are not persuasive.

Applicant argues that Ishibashi does not teach the limitation first set and second set each comprises at least two circuit units.

Examiner disagrees. 71A has plural elements mentioned in line 47 of column 1. Each element comprises one circuit unit. Thus, 71A has plural circuit units. Lines 56-59 of column 1 mention that the steps similar to 70A are performed in 70C. Thus, 71C has plural elements that are fed with clock 75C.

Applicant further argues that Ishibashi does not teach PLLs on the circuit board. Instead, PLLs are on the integrated circuit.

Examiner disagrees. Applicant agrees that integrated circuits are arranged on circuit board. As PLLs are on integrated circuits, PLLs are on circuit board too.

### **Conclusion**

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a). A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the

Art Unit: 2116

event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fahmida Rahman whose telephone number is 571-272-8159. The examiner can normally be reached on Monday through Friday 8:30 - 5:30. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2116

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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Art Unit 2116



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9/17/07